

CLAIMS

We claim:

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1. An apparatus for scheduling a Data Memory Access (DMA) having multiple channels, comprising:
- a shift structure having a plurality of entries corresponding to the multiple channels to be scheduled, wherein each entry in said shift structure includes a plurality of fields, and wherein each entry includes a weight that is determined based on said plurality of fields; and
- a comparison-logic circuit configured to sort said entries based on their respective weights.
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2. The apparatus of claim 1, wherein said comparison-logic circuit is configured to compare the weight of an entry being written into said shift structure with the weight of said entries in said shift structure.
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3. The apparatus of claim 2, wherein said comparison-logic circuit is configured to insert said entry being written into said shift structure behind entries with higher weights and to shift entries with lower weights behind said entry being written into said shift structure.
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4. The apparatus of claim 1, wherein said weight includes a number having a plurality of bits, and wherein each of said plurality of fields are assigned to a set of bits of said weight.

an enable field, wherein said enable field is assigned to the-most-significant bit of said weight;

an input-ready field, wherein said input-ready field is assigned to the third-most-significant bit of said weight;

a priority field, wherein said priority field is assigned to the fifth-most significant bit to the tenth-most significant bit of said weight.

7. The apparatus of claim 6, wherein the channels of the DMA are connected to a synchronized optical network (SONET) having a plurality of optical carrier (OC) numbers, and wherein said plurality of entries are assigned priority levels corresponding to the OC numbers of the channels associated with said plurality of entries.

8. The apparatus of claim 7, wherein:

a first set of entries associated with channels operating at OC 12 are assigned a priority level of 12; and

a second set of entries associated with channels operating at OC 3 are assigned a priority level of 3.

9. The apparatus of claim 1, wherein said shifting structure is a First-In-First-Out (FIFO) device.

10. A method of scheduling multiple channels on a Data Memory Access (DMA), comprising:

writing a plurality of entries in a shift structure, wherein each entry is associated with a channel on the DMA, and wherein each entry includes a plurality of fields;

assigning weights to said entries based on said plurality of fields;

15 sorting said entries based on said weights, wherein an entry having the highest weight is sorted to the head of said shift structure; and

reading said entry from the head of said shift structure to service the channel associated with said entry.

20 11. The method of claim 10 further comprising the step of:

writing said entry read from the head of said shift structure back into said shift structure after the channel associated with said entry is serviced.

12. The method of claim 11, wherein said writing step further comprises:

inserting said entry back into said shift structure behind entries in said shift

structure with higher weights; and

shifting said entries in said shift structure with lower weights behind said entry to

5 be written back.

13. The method of claim 10, wherein said weight includes a number having a plurality of bits, and said assigning step further comprises:

assigning each of said plurality of fields to a set of bits of said weight.

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14. The method of claim 13, wherein said plurality of fields includes:

an enable field, wherein said enable field is assigned to the-most-significant bit of said weight;

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an output-ready field, wherein said output-ready field is assigned to the second-most-significant bit of said weight;

an input-ready field, wherein said input-ready field is assigned to the third-most-significant bit of said weight;

an in-flight field, wherein said in-flight field is assigned to the fourth-most significant bit of said weight; and

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a priority field, wherein said priority field is assigned to the fifth-most significant bit to the tenth-most significant bit of said weight.

enabling said input-ready field of an entry when the channel associated with said entry is to be serviced.

assigning higher weights to higher priority levels.

assigning priority levels corresponding to the OC numbers of the channels.

assigning a priority level of 3 to a second set of entries associated with channels
ng at OC 3.

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sorting said entries based on said weights, wherein an entry having the highest weight is sorted to the head of said shift structure;

reading said entry from the head of said shift structure;

servicing the channel associated with said entry read from said shift structure; and

5 writing said entry read from said shift structure back into said shift structure.

20. The method of claim 19, wherein said writing step further comprises:

inserting said entry back into said shift structure behind entries in said shift structure with higher weights; and

10 shifting said entries in said shift structure with lower weights behind said entry to be written back.

21. The method of claim 19, wherein said weight includes a number having a plurality of bits, and said assigning step comprises:

15 assigning each of said plurality of fields to a set of bits of said weight.

22. The method of claim 19, wherein said plurality of fields includes a priority field having a plurality of priority levels.

20 23. The method of claim 22, wherein the channels are connected to a synchronized optical network (SONET) having a plurality of optical carrier (OC) numbers, and further comprising the step of:

assigning priority levels corresponding to the OC numbers of the channels.

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24. The method of claim 23 further comprising the steps of:

assigning a priority level of 12 to a first set of entries associated with channels
operating at OC 12; and

5 assigning a priority level of 3 to a second set of entries associated with channels
operating at OC 3.

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